CLOCK SYNCHRONIZED NONVOLATILE MEMORY DEVICE

The present application is a continuation of application Serial No. 10/223,220, filed August 20, 2002; which is a continuation of application Serial No. 10/020,873, filed December 19, 2001, now U.S. Patent No. 6459614; which is a continuation of application Serial No. 09/817,021, filed March 27, 2001, now U.S. Patent No. 6,366,495; which is a continuation of application Serial No. 09/583,949, filed May 31, 2000, now U.S. Patent No. 6,256,230; which is a continuation of application Serial No. 09/287,187, filed April 6, 1999, now U.S. Patent No. 6,111,790; which is a continuation of application Serial No. 09/053,494, filed April 2, 1998, now U.S. Patent No. 6,038,165; which is a continuation of application Serial No. 08/860,793, filed July 9, 1997, now U.S. Patent No. 5,889,698.

TECHNICAL FIELD

The present invention relates to a technique which is especially effective when applied to a multi-value data storing system in a semiconductor memory device and a nonvolatile semiconductor memory device, for example, to a technique which is effective when applied to a nonvolatile memory device (hereinafter referred to as the 'flash memory") for batch-erasing a plurality of memory data electrically.

BACKGROUND OF THE INVENTION

A flash memory uses nonvolatile memory elements each having a control gate and a floating gate similar to FAMOSs, as its memory cells, and